UNITED STATES PATENT APPLICATION FOR

AIRDOME ENCLOSURE FOR COMPONENTS

Inventors:
John S. Wei
Ray M. Parkhurst
Philip G. Nikkel
Michael J. Jennison

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BACKGROUND

A variety of components, e.g. electronic components and mechanical components, may include a coating of material for protecting the component from its external environment. For example, an electronic component may be applied with a plastic molding material during manufacture that provides moisture protection for the electronic component as well as provide electrical isolation among subcomponents of the electronic component.

A protective coating material on an electronic component may possess dielectric properties that may adversely affect the operation of the electronic component. For example, a plastic molding material may have a relatively high dielectric constant. A material with a relatively high dielectric constant may cause the formation of relatively high parasitic capacitances among the subcomponents of an electronic component. Unfortunately, high levels of parasitic capacitances among the subcomponents of an electronic component may adversely affect the operation of the electronic component. For example, parasitic capacitances may adversely affect the frequency response of an electronic component.

One prior technique for minimizing the undesirable parasitic capacitances in an electronic component caused by a protective coating is to employ a coating material having a relatively low dielectric constant. For example, composite materials or porous plastic materials having a relatively low dielectric

constant may be employed to protect an electronic component. Unfortunately, composite materials and porous plastic materials may increase the costs of manufacturing an electronic component by imposing additional steps on the manufacturing process.

SUMMARY OF THE INVENTION

A component is disclosed having an airdome enclosure that protects the component from its external environment. An airdome enclosure according to the present techniques avoids the high costs of employing special materials and/or specialized process steps in the manufacture of a component.

An electronic component according to the present technique includes a set of substructures for the electronic component formed on a substrate and an airdome enclosure over the substructures that protects the electronic component. The airdome enclosure includes air spaces that isolate the substructures while hindering the formation of parasitic capacitances among the substructures.

Other features and advantages of the present invention will be apparent from the detailed description that follows.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is described with respect to particular exemplary embodiments thereof and reference is accordingly made to the drawings in which:

Figures 1a-1b illustrate the formation of an electronic component that includes an airdome enclosure according to the present teachings;

Figure 2 is a cut-away perspective view of an electronic component that shows a set of dielectric regions that form seals in the gaps;

Figure 3 shows an embodiment that includes a pair of valleys formed in a top substructure that impede movement of dielectric material into the air spaces.

DETAILED DESCRIPTION

Figures 1a-1b illustrate the formation of an electronic component 10 that includes an airdome enclosure according to the present teachings. The airdome enclosure of the electronic component 10 protects the electronic component 10 and forms a set of air spaces 29 and 30 that provide electrical isolation among the subcomponents of the electronic component 10. The relatively low dielectric constant associated with the air in the air spaces 29 and 30 hinder the formation of undesirable parasitic capacitances among the subcomponents of the electronic component 10.

The electronic component 10 is formed onto a substrate 11. Example materials for the substrate 11 include silicon and gallium-arsenide. Other substrate materials include metal, plastic, circuit board materials, organic film, etc.

The electronic component 10 includes a series of layers deposited onto the substrate 11. The layer materials deposited onto the substrate 11 may be selected and patterned into the particular subcomponents for the electronic component 10. For example, the layers may be deposited and patterned to form transistor subcomponents, capacitor subcomponents, resistor subcomponents, etc., depending on the particular design of the electronic component 10. The materials of these layers may include any combination of metal and dielectric materials.

In one embodiment, the series of layers deposited onto the substrate 11 include a first, a second, and a third metal layer. Example methods for forming the metal layers include evaporation, sputtering, and plating.

The first metal layer is patterned into a set of metal structures 12, 13, and 14. The second metal layer is patterned into a set of metal structures 15 and 16.

A dielectric material is deposited over the metal structures 12-16 and patterned to form what will be the air spaces 29 and 30 and then the third metal layer is deposited over the dielectric material that covers the metal structures 12-16. The third metal layer is then patterned into a set of metal structures 17, 18, and 19. The dielectric material is then removed to reveal the air spaces 29 and 30. The dielectric material deposited over the metal structures 12-16 and patterned to form what will be the air spaces 29 and 30 may be a photo-resist or some other type of dielectric material.

The patterning of the third metal layer forms a ledge 20 on the structure 17 and a ledge 21 on the structure 18 with an air gap 40 in between the ledges 20 and 21. The patterning of the third metal layer also forms a ledge 22 on the structure 18 and a ledge 23 on the structure 19 with an air gap 42 in between the ledges 22 and 23. The air gaps 40-42 may be formed to the most narrow possible gap width given

the process technology used to form the electronic component 10. In one embodiment, the width of each air gap 40-42 is between 1 and 3 microns.

A dielectric overcoat is then deposited onto the electronic component 10 to form a set of dielectric films 26-28. The dielectric films 26-28 form a seal 70 in the air gap 40 and a seal 72 in the air gap 42 but do not fill in the air spaces 29-30. Example materials for the dielectric overcoat include silicon-dioxide, silicon-nitride, or a combination of silicon-dioxide and silicon-nitride, a plastic molding compound, or an organic molding compound.

The dielectric overcoat may be deposited using a dry process in which a gas reaction is used to form the dielectric material. The dielectric overcoat may be deposited using a wet process in which a liquid form of glass is applied and then heated. The dielectric overcoat may be formed by depositing an organic film followed by a curing step.

The width and/or shapes of the air gaps 40-42 may be selected to allow the dielectric overcoat to form the seals 70-72 while preventing the dielectric overcoat from entering and filling the air spaces 29 and 30. The widths and/or shapes of the air gaps 40-42 may be selected in response to the viscosity of the dielectric overcoat during deposition and/or the process temperature during deposition. The air spaces 29 and 30 may be filled with a air or low pressure gases during the deposition of the dielectric overcoat.

Figure 2 is a cut-away perspective view of the electronic component 10 that shows a set of dielectric regions 50-52 of the dielectric overcoat that form seals in the air gaps 40-42. This view also shows a set of dielectric regions 60-64 that form seals in openings on the top of the metal structure 18. The openings on the top of the metal structure 18 may be formed during cleanout of process material.

Figure 3 shows an embodiment in which the third metal layer includes a pair of valleys 80-82. The valleys 80-82 are shaped so as to impede the movement of dielectric material through the air gaps 40-42 into the air spaces 29 and 30 during formation of the dielectric overcoat. As before, the dielectric material underneath the third metal layer is removed after patterning of the air gaps 40-42 to reveal the air spaces 29 and 30.

The valleys 80-82 may be shaped by shaping the dielectric material, e.g. a photo-resist, underneath the third metal layer. For example, the V-shaped dips of the valleys 80-82 may be formed with a photo-masking step and exposure of the photo-resist. Alternatively, a single photo-mask may be employed with specially designed aperture patterns using OPC (Optical Proximity Correction) algorithms. If a dielectric material is used underneath the third metal layer then that dielectric material may be subjected to a second photo-masking and etching to produce the V-shaped dips for the valleys 80-82.

An airdome enclosure according to the present techniques may be used in any type of electronic component including active components and passive components. In addition, an airdome enclosure according to the present techniques may be used for any component, electronic or otherwise, that may benefit from the protection provided from an external environment.

The foregoing detailed description of the present invention is provided for the purposes of illustration and is not intended to be exhaustive or to limit the invention to the precise embodiment disclosed. Accordingly, the scope of the present invention is defined by the appended claims.